IN THE CLAIMS

Please amend the claims to the following:

1. (Currently Amended) A method comprising:

receiving a plurality of ~~partial data~~ write transactions with a controller hub from a requesting device, each of the plurality of ~~partial data~~ write transactions being associated with ~~including~~ a write combinable attribute to indicate they are a plurality of write combinable ~~partial data~~ write transactions;

buffering ~~combining partial~~ data associated with the plurality of ~~partial data~~ write combinable write transactions in a buffer of the controller ~~an input/output (I/O)~~ hub ~~to form write combined data~~ in response to each of the plurality of ~~partial data~~ write transactions being associated with ~~including~~ the write combinable attribute to indicate they are write combinable ~~partial data~~ write transactions; and

transmitting a write completion signal corresponding to each of the plurality of write combinable write transactions with the controller hub to the requesting device in response to buffering data associated with each of the plurality of write combinable write transactions;

flushing the data associated with the plurality of write combinable write transactions in the buffer as ~~the~~ write combined data ~~associated with the plurality of write transactions~~ to an I/O device in response to receiving a flush signal from the requesting device after transmitting the write completion signal corresponding to each of the plurality of write combinable write transactions.

2. (Currently Amended) The method of claim 1, wherein the requesting device is to transmit the flush signal in response to receiving a last write completion corresponding to a last write combinable write transaction of the plurality of write combinable write transactions ~~flushing the data to the I/O device includes: determining whether a flush signal has been received from a processor; and flushing the data if the flush signal has been received, the protocol including an signaling protocol~~.

3. (Currently Amended) The method of claim 2, wherein the write completion signal corresponding to each of the plurality of write transactions is transmitted by the controller hub before the requesting device transmits the flush signal, and wherein the controller hub is further to transmit a flush completion signal to the requesting device in response to flushing the data to the I/O device ~~further including sending a write completion signal to the processor for each of the plurality of partial data write transactions before the data is flushed to the I/O device, wherein each write completion signal is to verify buffering of a corresponding partial data write transaction of the plurality of partial data write transactions~~.

4. (Currently Amended) The method of claim 3, wherein the requesting device is not to issue any further write combinable writes to a same memory region associated with the plurality of write combinable writes from when the flush signal is transmitted by the requesting device to when the requesting device receives the flush completion signal ~~further including sending a flush completion signal to the processor after the data is flushed to the I/O device~~.

5. (Currently Amended) The method of claim 1 [[2]], wherein flushing the data as write combined data to the I/O device in response to receiving ~~if~~ the flush signal from the requesting

device ~~has been received~~ further includes:

tagging the buffer with a first source identifier associated with one or more of the write combinable write transactions and the requesting device;

detecting a second source identifier associated with the flushing signal;

comparing the second source identifier to the first source identifier; and

flushing the data as write combined data to the I/O device in response to ~~if~~ the second source identifier matching[[es]] the first source identifier.

6. (Original) The method of claim 5, further including repeating the comparing for a plurality of buffers, each buffer corresponding to an I/O port.

7. - 9. (Canceled).

10. (Currently Amended) The method of claim 1, wherein the write combined data includes ~~flushing the data to the I/O device includes flushing~~ more than one cache line worth of data ~~to the I/O device~~.

11. (Original) The method of claim 1, wherein the receiving includes receiving a plurality of commands instructing the I/O hub to consider each write transaction for write combining, each of the plurality of write transactions including one of the plurality of commands.

12. (Currently Amended) An ~~input/output (I/O) hub~~ apparatus comprising:

a hub to be coupled to a processor, the hub including:

receiving logic to receive a first write transaction and a second write transaction from a processor, the first and the second write transactions to reference partial data of a cache line within the processor, wherein the first and second write transactions include a write combinable attribute to indicate the first and the second partial write transactions as write combinable,

combining logic coupled to the receiving logic to combine the partial data of the cache line referenced by the first and second write transactions as write combined data in response to the first and second write transactions including the write combinable attribute to indicate they are write combinable; and

flushing logic coupled to the combining logic to flush the write combined data to an I/O device in response to a protocol event.

13. (Currently Amended) The apparatus ~~I/O hub~~ of claim 12, wherein the protocol event includes special flush signal to be received by the receiving logic from the processor.

14. (Currently Amended) The apparatus ~~I/O hub~~ of claim 13, further comprising transmission logic to send a first and a second write completion signal to the processor for the first and the second write transactions, respectively, before the write combined data is flushed to the I/O device, wherein the first and the second write completion signals are to verify successful storage of the partial data referenced by the first and the second write transactions, respectively.

15. (Currently Amended) The apparatus ~~I/O hub~~ of claim 14, wherein the transmission logic is also to send a flush completion signal to the processor after the write combined data is flushed to the I/O device.

16. (Currently Amended) The apparatus ~~I/O hub~~ of claim 12, further comprising latency logic coupled to the combining logic to detect occurrence of ~~determine whether~~ a latency condition ~~exists~~, wherein the protocol event includes occurrence of the latency condition.

17. (Currently Amended) The apparatus ~~I/O hub~~ of claim 16, further comprising transmission logic to send a first and a second write completion signal to the processor for the first and the second write transactions, respectively, as the write combined data is flushed to the I/O device, wherein the first and the second write completion signals are to verify flushing of the first and the second write transactions, respectively.

18. (Currently Amended) The apparatus ~~I/O hub~~ of claim 16, wherein the latency condition includes a delay in receiving a next third combinable write transaction from the processor and an interface to the I/O device being in an idle state.

19. (Currently Amended) The apparatus ~~I/O hub~~ of claim 12, wherein the combining logic includes a plurality of buffers, each buffer corresponding to an I/O port, and wherein the flushing logic is to flush data from one of the plurality of buffers corresponding to the processor in response to a protocol event associated with the processor.

20. (Cancelled).

21. (Currently Amended) An apparatus ~~system~~ comprising:

a hub to be coupled to a first device and a second, the hub including:

a buffer;

receiving logic to receive a first combinable write transaction and a second combinable write transaction from the first device; and

a write combining module to

store first data associated with the first combinable write transaction in the buffer and send a first write completion signal to the first device in response to storing the first data in the buffer,

store second data associated with the second combinable write transaction in the buffer and send a second write completion signal to the first device in response to storing the second data in the buffer, and

flush the first data and the second data as combined data to the second device in response to receiving a flush signal from the first device.

~~an input/output (I/O) device;~~

~~a processor to associate a write combinable attribute with a plurality of write transactions to identify them as write combinable and to transmit the plurality of write transactions, wherein each of the write transactions are to be associated with partial data; and~~

~~an I/O hub coupled to the I/O device s and the processor, the I/O hub having a write combining module to receive the plurality of write transactions from the processor, to combine the partial data associated with the plurality of write transactions to form a write combined data set in response to the plurality of write transactions being associated with the write combinable attribute to identify them as write combinable,~~

~~and to transmit the write combined data set to the I/O device in response to a protocol event associated with the processor~~.

22. (Currently Amended) The apparatus ~~system of~~ claim 21, wherein the first device includes a processor and the second device include an input/output (I/O) device ~~the protocol event includes a flush signal from the processor~~.

23. (Currently Amended) The apparatus ~~system of~~ claim 22, wherein the processor is to generate the flush signal in response to a flushing event, the flushing event being selected from a group consisting of use of an ordering fence, encountering an implicit locked instruction, and encountering an interrupt ~~occuring and a write combine history indicating that one or more combinable write transactions have been issued by the processor~~.

24. (Currently Amended) The apparatus ~~system of~~ claim 23, wherein the processor is to generate the flush signal further in response to a write combine history indicating the first combinable write transactin and the second write combinable transaction have been issued by the processor ~~the write combine history is to track combinable write transactions for a particular processor thread~~.

25. (Currently Amended) The apparatus ~~system of~~ claim 22 [[24]], wherein the write combining[[e]] module is further to send a flush completion signal to the processor in response to the flush of the first data and the second data as combined data to the I/O device. ~~history is to further track combinable write transactions for a particular I/O hub~~.

26. (Currently Amended) The apparatus ~~system of~~ claim 25 [[22]], wherein the processor is not to issue any further write combinable write transactions to a memory region associated with the firs and the second combinable write transactions from when the processor generates the flush signal to when the processor receives the flush completion signal ~~the I/O hub is included in a chipset that includes a plurality of I/O hubs, the processor to send the flush signal to each of the plurality of I/O hubs~~.

27. (Currently Amended) The apparatus ~~system of~~ claim 22 [[26]], wherein the write combining module is to be implemented in a layered communication protocol including at least a physical layer and a link layer. ~~the processor is to verify that one or more combinable write transactions have been sent to each of the plurality of I/O hubs before sending the flush signal~~.

28. (Currently Amended) The apparatus ~~system of~~ claim 27 [[21]], wherein the hub is to be coupled to the processor though a point-to-point interconnect ~~the protocol event includes a latency condition~~.

29. (Currently Amended) The apparatus ~~system of~~ claim 21, wherein the write combining module is further to flush the first data and the second data as combined data to the second device in response to receiving a flush signal from the first device comprises: determine the flush signal is from the first device based on a first source identifier associated with the first and second combinable write transactions matching a second source identifier associated with the flush signal ~~the processor is to instruct the I/O hub to consider each write transaction for write combining based on a page table attribute associated with the write transactions~~.

30. (Cancelled)

31. (Currently Amended) A method comprising:

receiving a plurality of write transactions from a processor with a controller hub, the plurality of write transactions being identified as write combinable transactions and being destined for a[[n input/output (I/O)]] device coupled to the controller hub;

storing data associated with the plurality of write transactions to a buffer of the controller hub ~~I/O~~ hub in response to the plurality of write transactions being identified as write combinable transactions;

determining whether a latency condition exists, the latency condition including at least a delay in receiving a next combinable write transaction from the processor ~~and an interface to the I/O device being in an idle state~~;

flushing the data to the I/O device in response to determining ~~if~~ the latency condition exists; and

sending a write completion signal to the processor for each of the plurality of write transactions in response to ~~as~~ the data being ~~is~~ flushed to the ~~I/O~~ device~~, each write completion signal verifying flushing of a corresponding write transaction~~.

32. (Currently Amended) The method of claim 31, wherein the device includes an input/output (I/O device, flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device, and the latency condition further comprises an interface to the I/O device being idle..

33. (Currently Amended) The method of claim 31, wherein the receiving includes receiving a plurality of commands instructing the controller ~~I/O~~ hub to consider each write transaction for write combining, each of the plurality of write transactions including one of the plurality of commands.

34. (Currently Amended) An apparatus comprising:

a processor including:

write logic to transmit a plurality of write transactions to be identified as write combinable to a hub;

receiving logic to receive a write completion for each of the plurality of write transactions from the hub;

protocol logic to transmit a flush signal to the hub to initiate a flush of data associated with the plurality of write transactions in response to detecting a flush event and receiving, with the receiving logic, a last write completion for a last write transaction of the plurality of write transactions.

~~page table logic to identify a page in a memory; wherein the page table logic is to associate a write combining attribute with the page in the memory to indicate that partial writes from the page are combinable; write combining logic to combine a plurality of partial writes from the page into a combined write in response to the write combining attribute associated with the write combining attribute to indicate that partial writes from the page are combinable; and transmit logic to transmit the combined write to an external device~~.

35. (Currently Amended) The apparatus of claim 34, wherein the flush event is selected from a group consisting of use of an ordering fence, encountering an implicit locked instruction, and encountering an interrupt ~~the plurality of partial writes include partial writes of a cache line, and wherein the combined write includes a full cache line~~.

36. (Currently Amended) The apparatus of claim 34, wherein the protocol logic is further to not allow the write logic to transmit any further write transactions to be identified as write combinable to a memory region associated with the plurality of write transactions from when the protocol logic transmits the flush signal to when the receiving logic receives a flush completion signal from the hub to indicate the flush of the data associated with the plurality of write transactions has been performed ~~the external device includes an input/output (I/O) device to be coupled to the apparatus utilizing a point-to-point interconnect~~.

37. (New) An apparatus comprising:

a hub to be coupled to a processor and a device including:

receiving logic to receive a plurality of combinable write transactions from the processor;

a buffer to store data associated with the plurality of combinable write transactions;

latency detection logic to detect occurrence of a latency condition, the latency condition including at least a delay in receiving a next combinable write transaction from the processor;

flushing the data associated with the plurality of combinable write transactions to the device in response to the latency detection logic detecting the latency condition; and

protocol logic to send a write completion signal to the processor for each of the plurality of write transactions in response to the data being flushed to the device.

38. (New) The method of claim 37, wherein the device includes an input/output (I/O) device, the hub includes an I/O hub, flushing the data to the I/O device includes flushing more than one cache line worth of data to the I/O device, and the latency condition further comprises an interface to the I/O device being idle.

39. (New) The method of claim 37, wherein the processor is not to send any further combinable write transactions from when a flush event is detected by the processor until when the processor receives a last completion signal from the hub corresponding to a last combinable write transaction of the plurality of combinable write transactions.